Title (en)

Microprocessor system for an electronic postage arrangement

Title (de)

Mikroprozessorsystem für eine elektronische Frankieranordnung

Title (fr)

Système à microprocesseur pour arrangement d'affranchissement électronique

Publication

EP 0736846 B1 20001025 (EN)

Application

EP 96110413 A 19830125

Priority

- EP 92114140 A 19830125
- EP 86116058 A 19830125
- US 34387782 A 19820129

Abstract (en)

[origin: EP0085385A2] An electronic postage meter has an accounting unit with redundant nonvolatile random access memories (20, 21) controlled by a microprocessor (10). The redundant random access memories (20, 21) have separate groups of address (22, 24) and data lines (23, 25) to minimize identical errors in data stored therein. Data transfer may occur at different times to and from the memories, with respect to any given byte of data. The system may incorporate redundant microprocessors, and critical parameters may be checked at periodic intervals in the main program of the accounting microprocessor system.

[origin: EP0085385A2] The system has a microprocessor connected to a number of address lines, data lines, and control lines. A memory unit is connected to the address and data lines and to the control lines to enable storage of data in the memory, and reading of data from, under the control of the microprocessor. The memory unit comprises two RAMs each connected to separate groups of the address lines and separate groups of the data lines. The data may be transferred to and from the two RAMs independently of any common interconnection. In this way the possibility of error conditions that are not detectable is reduced.

IPC 1-7

G07B 17/02

IPC 8 full level

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CPC (source: EP)

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