

Publication

EP 0744712 A3 19961211

Application

EP 96303710 A 19960524

Priority

JP 12538495 A 19950524

Abstract (en)

[origin: EP0744712A2] This texture pattern memory circuit is composed of a multi-texture pattern memory 2A, a writing device 3A and a texel selector 4A. The multi-texture pattern memory 2A includes an adder 5A, a subtracter 6A, selectors 7A and 8A, 1st to 4th address converting devices 9A1 through 9A4, and 1st to 4th memory modules 10A1 through 10A4. The texel selector 4 selects only the necessary data from the texel data outputted from the multi-texture pattern memory 2A. <IMAGE>

IPC 1-7

G06T 15/10

IPC 8 full level

G06F 12/00 (2006.01); **G06F 12/06** (2006.01); **G06T 1/60** (2006.01); **G06T 11/20** (2006.01); **G06T 15/00** (2006.01); **G06T 15/20** (2006.01); **G09G 5/39** (2006.01)

CPC (source: EP US)

G06T 15/04 (2013.01 - EP US)

Citation (search report)

- [A] GB 2267203 A 19931124 - FUJITSU LTD [JP]
- [A] "SHARED TEXTURE MAP MEMORY IN A MULTI-RASTERIZER SYSTEM", IBM TECHNICAL DISCLOSURE BULLETIN, vol. 37, no. 06A, June 1994 (1994-06-01), NEW YORK US, pages 269 - 275, XP000455768

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EP 0744712 A2 19961127; **EP 0744712 A3 19961211**; **EP 0744712 B1 20021120**; DE 69624866 D1 20030102; DE 69624866 T2 20031009; JP 3081774 B2 20000828; JP H08320946 A 19961203; US 5877770 A 19990302

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