

Title (en)

Method of forming raised source/drain regions in an integrated circuit

Title (de)

Verfahren zur Bildung von erhöhten Source- und Drainzonen in integrierten Schaltungen

Title (fr)

Méthode pour former des régions de source/drain saillantes dans un circuit intégré

Publication

**EP 0747941 A3 19980722 (EN)**

Application

**EP 96303952 A 19960531**

Priority

US 48634795 A 19950607

Abstract (en)

[origin: EP0747941A2] A method is provided for forming a planar transistor of a semiconductor integrated circuit, and an integrated circuit formed according to the same. A plurality of field oxide regions are formed overlying a substrate electrically isolating a plurality of transistors encapsulated in a dielectric. LDD regions are formed in the substrate adjacent the transistors and the field oxide regions. Doped polysilicon raised source and drain regions are formed overlying the LDD regions and a tapered portion of the field oxide region and adjacent the transistor. These polysilicon raised source and drain regions will help to prevent any undesired amount of the substrate silicon from being consumed, reducing the possibility of junction leakage and punchthrough as well as providing a more planar surface for subsequent processing steps. <IMAGE>

IPC 1-7

**H01L 21/336**; **H01L 21/285**

IPC 8 full level

**H01L 21/28** (2006.01); **H01L 21/285** (2006.01); **H01L 21/336** (2006.01); **H01L 21/8234** (2006.01); **H01L 27/088** (2006.01); **H01L 29/08** (2006.01); **H01L 29/417** (2006.01); **H01L 29/45** (2006.01); **H01L 29/78** (2006.01)

CPC (source: EP US)

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Citation (search report)

- [Y] EP 0422824 A1 19910417 - AMERICAN TELEPHONE & TELEGRAPH [US]
- [XY] PATENT ABSTRACTS OF JAPAN vol. 014, no. 145 (E - 0905) 19 March 1990 (1990-03-19)

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