Title (en)

A HIGH-SPEED LATCH CIRCUIT INCLUDING MULTIPLE TRANSMISSION GATES AND A PIPELINED MICROPROCESSOR EMPLOYING THE SAME

Title (de)

SCHNELLE VERRIEGELUNGSSCHALTUNG, DIE MEHREREN ÜBERTRAGUNGSGATTERN ENTHÄLT UND PIPELINE-MIKROPROZESSOR DER DIESELBE VERWENDET

Title (fr)

CIRCUIT DE VERROUILLAGE HAUTE VITESSE COMPRENANT DES GRILLES DE TRANSMISSION ET MICROPROCESSEUR PIPELINE METTANT EN OEUVRE CE CIRCUIT

Publication

EP 0752174 A1 19970108 (EN)

Application

EP 96903546 A 19960122

Priority

- US 9600676 W 19960122
- US 37786495 A 19950125
- US 37817595 A 19950125

Abstract (en)

[origin: WO9623355A1] A latch circuit is provided wherein a first transmission gate is electrically coupled in series with a second transmission gate between an input line and an output line. The latch circuit is controlled by a single clock signal wherein a delay element is employed to simultaneously enable both transmission gates upon an edge of the clock signal. The length of time during which both transmission gates are enabled is determined by an electrical delay associated with the delay element. When both transmission gates are enabled, the input line is electrically coupled to the output line. A keeper circuit at the output of the second transmission gate retains a logical value at the output of the latch after the input line is decoupled from the output line. In one implementation, the delay element is implemented with a set of serially coupled inverters, and the length of the time delay controls the time window during which both transmission gates are enabled. The latch circuit may be employed between pipeline stages in a processor.

IPC 1-7

H03K 3/037; G06F 9/38

IPC 8 full level

G06F 9/38 (2006.01); **H03K 3/037** (2006.01)

CPC (source: EP)

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