Title (en)

Circuit for generating a bias voltage

Title (de

Schaltungsanordnung zur Erzeugung eines Biaspotentials

Title (fr)

Circuit pour générer une tension de polarisation

Publication

EP 0766163 B1 19990421 (DE)

Application

EP 96114180 A 19960904

Priority

DE 19535807 A 19950926

Abstract (en)

[origin: DE19535807C1] The circuit includes a first transistor (2) with its collector connected to a supply potential (1). A first resistor (3) is connected between the base and the collector of the transistor (2). A first current source (5) is connected between the base of the first transistor (2) and a reference potential (4). A second current source (6) is connected between the emitter of the first transistor (2) and the reference potential (4). A second transistor (7) has its base connected to the supply potential (1). Its base is connected to the emitter of the first transistor (2). A third current source (8) is connected between the emitter of the second transistor (7) and the reference potential (4). A third transistor (9) conducts the bias potential at its collector. A second resistor (10) is connected between the emitter of the second transistor (7) and the base of the third transistor (9). A third resistor (11) is connected between the collector of the third transistor (9) and the supply potential (1). A first forward biased diode (12) is connected between the base of the third transistor (9) and the reference potential (4). A fourth resistor (13) is connected between the emitter of the third transistor (9) and the reference potential (4). The fourth resistor (13) has a resistance half of that of the second or third resistors (10,11), which are the same size as each other. The second and third current sources supply a current dependent on the collector current of the third transistor (9).

IPC 1-7

G05F 3/20; G05F 3/22

IPC 8 full level

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CPC (source: EP US)

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