

Title (en)
Memory device for digital picture signal

Title (de)
Speichervorrichtung für ein digitales Bildsignal

Title (fr)
Dispositif de mémoire pour un signal numérique d'image

Publication
EP 0767587 A3 19990616 (EN)

Application
EP 96307209 A 19961002

Priority
• JP 27834995 A 19951002
• JP 28465595 A 19951005

Abstract (en)
[origin: EP0767587A2] In a memory apparatus, for use with a digital picture signal, a signal processing means for processing an input digital picture signal on a real time basis, and a memory for storing output data of the processing means, are disposed on a common semiconductor substrate. The signal processing means performs a hierarchical encoding process for forming data in a second hierarchical level with an average value of every N pixels of data in a first hierarchical level, the input digital picture data being the data in the first hierarchical level. <IMAGE>

IPC 1-7
H04N 7/26

IPC 8 full level
H04N 7/26 (2006.01)

CPC (source: EP KR US)
G11C 7/00 (2013.01 - KR); **H04N 19/63** (2014.11 - EP US); **H04N 19/42** (2014.11 - EP US)

Citation (search report)
• [X] EP 0627859 A2 19941207 - SONY CORP [JP]
• [XA] WINZKER M ET AL: "VLSI CHIP SET FOR 2D HDTV SUBBAND FILTERING WITH ON-CHIP LINE MEMORIES", IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 28, no. 12, 1 December 1993 (1993-12-01), pages 1354 - 1361, XP000435910
• [A] GOLDBERG M ET AL: "COMPARATIVE PERFORMANCE OF PYRAMID DATA STRUCTURES FOR PROGRESSIVE IMAGE TRANSMISSION", IEEE TRANSACTIONS ON COMMUNICATIONS, vol. 39, no. 4, 1 April 1991 (1991-04-01), pages 540 - 547, XP000241265
• [A] QUEIROZ R L DE ET AL: "ON A HYBRID PREDICTIVE-INTERPOLATIVE SCHEME FOR REDUCING PROCESSING SPEED IN DPCM TV CODECS", 18 September 1990, SIGNAL PROCESSING THEORIES AND APPLICATIONS, BARCELONA, SEPT. 18 - 21, 1990, VOL. VOL. 2, NR. CONF. 5, PAGE(S) 797 - 800, TORRES L; MASGRAU E; LAGUNAS M A, XP000365713
• [A] JAVIER VEGA-PINEDA ET AL: "VLSI IMPLEMENTATION OF A WAVELET IMAGE COMPRESSION TECHNIQUE USING REPLICATED CODING/DECODING CELLS", 30 April 1995, 1995 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS), SEATTLE, APR. 30 - MAY 3, 1995, VOL. VOL. 2, PAGE(S) 1173 - 1176, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, XP000558881

Cited by
KR100635235B1; EP0895215B1

Designated contracting state (EPC)
DE FR GB IT

DOCDB simple family (publication)
EP 0767587 A2 19970409; EP 0767587 A3 19990616; EP 0767587 B1 20060517; DE 69636139 D1 20060622; DE 69636139 T2 20061130; DE 69636352 D1 20060824; DE 69636352 T2 20070628; EP 1065882 A1 20010103; EP 1065882 B1 20060712; KR 100445014 B1 20041112; KR 970023368 A 19970530; US 2001012404 A1 20010809; US 6873738 B2 20050329

DOCDB simple family (application)
EP 96307209 A 19961002; DE 69636139 T 19961002; DE 69636352 T 19961002; EP 00111790 A 19961002; KR 19960044209 A 19961002; US 72239596 A 19960930