Title (en)

A PIPELINED MICROPROCESSOR THAT MAKES MEMORY REQUESTS TO A CACHE MEMORY AND AN EXTERNAL MEMORY CONTROLLER DURING THE SAME CLOCK CYCLE

Title (de)

PIPELINEMIKROPROZESSOR, DER SPEICHERANFORDERUNGEN WÄHREND DESSELBEN TAKTZYKLUSES ZU EINEM CHACHESPEICHER UND ZU EINEM STEUERUNGSGERÄT EINES EXTERNEN SPEICHERS STELLT

Title (fr)

MICROPROCESSEUR PIPELINE EFFECTUANT DES REQUETES EN MEMOIRE DANS UNE MEMOIRE CACHE ET DANS UN CONTROLEUR DE MEMOIRE EXTERIEURE DURANT UN MEME CYCLE D'HORLOGE

Publication

EP 0772829 A1 19970514 (EN)

Application

EP 96920253 A 19960516

Priority

- US 9607091 W 19960516
- US 45230695 A 19950526

Abstract (en)

[origin: WO9637844A1] Memory requests are made to a cache memory and an external memory controller during the same clock cycle when the bus connected to the external memory is available. By making both memory requests during the same clock cycle rather than first accessing the cache memory as is conventionally done, the cycle time lost when the request is not stored in the cache memory can be eliminated. The unneeded external memory requests that result each time the request is stored in the cache memory are eliminated by gating the request to the external memory controller with a logic signal output by the cache memory that indicates whether the request is present.

IPC 1-7

G06F 12/08

IPC 8 full level

G06F 12/08 (2006.01); **G06F 12/0884** (2016.01)

CPC (source: EP KR)

G06F 12/08 (2013.01 - KR); **G06F 12/0884** (2013.01 - EP)

Citation (search report)

See references of WO 9637844A1

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

WO 9637844 A1 19961128; EP 0772829 A1 19970514; KR 970705086 A 19970906

DOCDB simple family (application)

US 9607091 W 19960516; EP 96920253 A 19960516; KR 19970700548 A 19970127