Title (en)

Method of compensating offset voltage caused in analog arithmetic unit and analog arithmetic unit

Title (de)

Verfahren zur Kompensation der in analoger Recheneinheit verursachten Offsetspannung und analoge Recheneinheit

Title (fr)

Procédé de compensation de tension de décalage provoqueé dans une unité arithmétique analogique et unité arithmétique analogique

Publication

EP 0789312 B1 20020925 (EN)

Application

EP 97300828 A 19970207

Priority

JP 2277996 A 19960208

Abstract (en)

[origin: EP0789312A1] An analog arithmetic unit furnished with an input capacitor, an amplifier, a floating gate MOS. An input voltage is given to the amplifier through the input capacitor. The amplifier is composed of a CMOS inverter or the like and has a floating gate in a node at its input end. The floating gate MOS controls an amount of charges in the above node by injecting the hot electrons or absorbing the charges through the tunnel effect. Accordingly, it has become possible to maintain an amount of charges at the above node at a constant level over a long period. Thus, a frequency at which an offset voltage caused by charges accumulated at the above floating gate and causing an operation error can be reduced, thereby increasing an overall arithmetic operation. <IMAGE> <IMAGE>

IPC 1-7

G06G 7/12

IPC 8 full level

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