Title (en)

A memory system with multiplexed input-output port and memory mapping capability and systems and methods using the same

Title (de)

Speicheranordnung mit multiplexiertem Ein-/Ausgangstor und mit Speicherabbildungsfähigkeit und System und Verfahren, die diese verwenden

Title (fr)

Système de mémoire à port d'entrée/sortie multiplexé et à capacité de mapage de mémoire et systèmes et procédés l'utilisant

Publication

EP 0803816 A2 19971029 (EN)

Application

EP 97301835 A 19970319

Priority

US 63707396 A 19960424

Abstract (en)

A memory 600 including an array of memory cells 201 and a plurality of input/output terminals 220 for receiving control bits during control cycles and accessing selected ones of the cells 201 during data access cycles. A command bit input terminal 221 is provided for receiving command bits for initiating the control cycles and a mapping input terminal 222 is provided for receiving a mapping enable signal to initiate a mapping mode. Circuitry 215/ 216 is provided for decoding control bits received during at least one control cycle occurring a mapping mode for allowing a mapping a set of addresses for accessing the cells of the array 201.

IPC 1-7

G06F 12/02

IPC 8 full level

G11C 11/401 (2006.01); **G06F 12/02** (2006.01); **G06F 12/06** (2006.01); **G11C 5/06** (2006.01)

CPC (source: EP US)

G06F 12/0292 (2013.01 - EP US); **G11C 5/066** (2013.01 - EP US)

Cited by

EP1158399A3; EP0957490A1; US6065093A; WO9931665A1; KR100332188B1

Designated contracting state (EPC)

BE DE ES FR GB IE IT NL

DOCDB simple family (publication)

EP 0803816 A2 19971029; **EP 0803816 A3 20010425**; JP H1074387 A 19980317; TW 325567 B 19980121; US 5835965 A 19981110

DOCDB simple family (application)

EP 97301835 A 19970319; JP 10023397 A 19970417; TW 86103304 A 19970317; US 63707396 A 19960424