

Title (en)

Circuit for generating a voltage reference which can be enabled and disabled

Title (de)

Ein-/Ausschaltbare Schaltungsanordnung zur Erzeugung eines Referenzpotentials

Title (fr)

Circuit pour générer une tension de référence pouvant être validée ou inhibée

Publication

EP 0809169 B1 20000809 (DE)

Application

EP 97107599 A 19970505

Priority

DE 19621110 A 19960524

Abstract (en)

[origin: DE19621110C1] The circuit has a first transistor coupled to a given potential at its emitter and a second transistor coupled in common base configuration with the first transistor. The collectors of both transistors are coupled to the output terminal for the reference potential via respective resistors. The emitter of the second transistor is coupled to the given potential via a further resistor, its collector coupled to the base of a third transistor connected at its collector to a controlled current source. The switching signal is fed to the base of a fifth transistor in parallel with the third transistor.

IPC 1-7

G05F 3/26; **G05F 3/30**

IPC 8 full level

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CPC (source: EP US)

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