Title (en)

Booster circuit and method of driving the same

Title (de)

Spannungserhöhungsschaltung und Betriebsverfahren dafür

Title (fr)

Circuit élévateur de tension et sa méthode d'entraînement

Publication

EP 0810720 A3 19991020 (EN)

Application

EP 97301785 A 19970318

Priority

JP 13312296 A 19960528

Abstract (en)

[origin: EP0810720A2] A typical booster circuit of the present invention comprises a first capacitor (C1) having first and second electrodes, a second capacitor (C2) having first and second electrodes, and a switching circuit (T1 to T4) for transferring boosted potential appearing on each first electrode of the first and second capacitors to a boosting potential output node (VOUT). A precharge circuit operates to precharge each first electrode of the first and second capacitors (C1,C2). A logic circuit (21) operates to set the potential level of the second electrode of the first capacitor (C1) to a first potential level and to set the potential level of the second electrode of the second capacitor (C2) to a second potential level which is higher than the first potential level, upon reception of a control signal (Sc) having a first state, and to set the potential level of the second electrode of the first capacitor (C1) to the second potential level, and to set the potential level of the second electrode of the second capacitor (C2) to the first potential level, upon reception of a control signal (Sc) having a second state. A detector circuit (13) outputs a detecting signal (Ss) having a first state when the potential level of the boosting potential output node (VOUT) is lower than a given value, and outputs a detecting signal (Ss) having a second state when the potential level of the boosting potential output node is higher than the given level. A control signal generator circuit (23) alternately outputs a control signal (Sc) having first and second states in response to an oscillation signal (OSC) upon reception of a detecting signal (Ss) having a first state, and for outputting either of the control signals (Sc) having the first state or the control signal (Sc) having the second state irrespective of the oscillation signal upon reception of a detecting signal (Ss) having a second state. <IMAGE>

IPC 1-7

H02M 3/07

IPC 8 full level

G11C 11/407 (2006.01); **H02J 1/00** (2006.01); **H02M 3/07** (2006.01)

CPC (source: EP KR US)

G11C 5/14 (2013.01 - KR); **H02M 3/073** (2013.01 - EP US)

Citation (search report)

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DE FR GB NL

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EP 0810720 A2 19971203; **EP 0810720 A3 19991020**; CN 1173023 A 19980211; JP H09320267 A 19971212; KR 100347355 B1 20021025; KR 970076800 A 19971212; TW 378324 B 20000101; US 5781426 A 19980714

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