Title (en)

ARCHITECTURE FOR EFFICIENT INTERPOLATOR

Title (de)

ARCHITEKTUR FÜR EINEN EFFIZIENTEN INTERPOLATOR

Title (fr)

ARCHITECTURE PERMETTANT D'OBTENIR UN INTERPOLATEUR EFFICACE

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Abstract (en)

[origin: WO9623264A1] An efficient architecture for an interpolator (100) disposed to process oversampled data is disclosed herein. The interpolator (100) includes an input divider circuit (104) configured to receive an input data word over an input data line. A register (108) is provided for latching the divided input data word from the divider (104). The divided input data word is added within a summer (112) to a latched divided data word from the register, thereby forming a summed data word. A multiplexer (116) produces an interpolated output by multiplexing the summed data word with an input data word. In a preferred implementation, the register (108) is latched at a first clock rate, and the multiplexer (116) is clocked at twice the first clock rate. The efficient filter architecture allows interpolation to be performed in the absence of multipliers, and in a manner using filter coefficients equivalent to powers of two. This enables the interpolator (100) to be realized inexpensively, and renders the filter particularly suitable for implementation within integrated circuits.

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