

Title (en)
Circuit for generating a voltage reference

Title (de)
Schaltungsanordnung zur Erzeugung eines Referenzpotentials

Title (fr)
Circuit pour générer une tension de référence

Publication
EP 0814396 A3 19981209 (DE)

Application
EP 97109351 A 19970609

Priority
DE 19624676 A 19960620

Abstract (en)
[origin: DE19624676C1] The circuit arrangement comprises a first transistor (T1), whose emitter is joined with a ground voltage (M) and whose basis and collector are connected with each other, and a second transistor (T2), whose basis is joined with the basis of the first transistor. A first resistance (R1) is connected between the collector of the first transistor and an output (U) for providing the reference voltage. A second resistance (R2), is connected between the collector of the second transistor and the output. A third resistance (R3) is connected between the emitter of the second transistor and the ground voltage. A third transistor (T3) is provided, whose basis is connected with the collector of the second transistor and whose emitter is joined with the ground voltage. A fourth transistor (T4) has its collector connected with supply voltage (V), its emitter connected to the output and its basis to the collector of the third transistor, whereby a first current source (R5, T5) is provided between basis and collector of the fourth transistor. A second current source (T17, R16) is connected in parallel to the first current source, for compensation of the current sway of the first current source.

IPC 1-7
G05F 3/26; **G05F 3/30**

IPC 8 full level
G05F 3/22 (2006.01); **G05F 3/26** (2006.01); **G05F 3/30** (2006.01)

CPC (source: EP US)
G05F 3/222 (2013.01 - EP US); **G05F 3/265** (2013.01 - EP US)

Citation (search report)

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