

Title (en)

PROCESS FOR FORMING A SPATIAL CHIP ARRANGEMENT, AND SAID SPATIAL ARRANGEMENT

Title (de)

VERFAHREN ZUR AUSBILDUNG EINER RÄUMLICHEN CHIPANORDNUNG UND RÄUMLICHE CHIPANORDNUNG

Title (fr)

PROCEDE DE CONFIGURATION D'UN SYSTEME SPATIAL DE PUCES ET SYSTEME SPATIAL DE PUCES CORRESPONDANT

Publication

**EP 0847597 A1 19980617 (DE)**

Application

**EP 97929104 A 19970614**

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Abstract (en)

[origin: DE19626126A1] The invention relates to a process for forming a spatial chip arrangement with a plurality of chips (32, 36, 37, 38, 39) connected by electrical means to each other and arranged in different planes. The chips are connected via the peripheral connection surfaces (33) thereof to associated strip conductors (23) of a strip conductor structure (24, 25) arranged on at least one carrier substrate (21, 22) in that the chips are either arranged transversely to the longitudinal extension of the carrier substrate or parallel to the longitudinal extension of the flexible carrier substrate. The invention also relates to a spatial chip arrangement formed by said process.

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IPC 8 full level

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DOCDB simple family (publication)

**DE 19626126 A1 19980102**; **DE 19626126 C2 19980416**; EP 0847597 A1 19980617; JP 3739013 B2 20060125; JP H11511910 A 19991012; KR 100595047 B1 20061130; KR 19990044229 A 19990625; US 2002009828 A1 20020124; US 6281577 B1 20010828; US 7087442 B2 20060808; WO 9800868 A1 19980108

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