

Title (en)

Isolation of PCI and EISA masters by masking control and interrupt lines

Title (de)

Isolierung von PCI- und EISA-Master mittels Maskierung von Steuerungs- und Unterbrechungsleitungen

Title (fr)

Isolation des maîtres PCI et EISA par masquage des lignes de commande et d'interruption

Publication

**EP 0851363 A2 19980701 (EN)**

Application

**EP 97310693 A 19971231**

Priority

US 77539296 A 19961231

Abstract (en)

A system management module (SMM) for a host server system includes a system management processor (SMP) connected to a system management local bus. The system management local bus connects to the system PCI bus through a system management central (SMC). The SMC includes the main arbitration unit for the PCI bus and also includes the arbiter for the system management local bus. The SMM includes a video controller and/or keyboard and mouse controller connected to the system management local bus to support remote consoling of the SMM. The SMC includes logic to monitor PCI cycles and to issue error signals in the event of a system error. The SMC also isolates failed components by masking request grant and interrupt lines for the failed device. Further, if a spare component is provided, the SMC permits dynamic switching to the spare. In addition to detecting errors and performing survival and maintenance operations, the SMC enhances system performance during normal operations by supporting master-target priority determinations to more efficiently arbitrate mastership of system busses such as the PCI bus. <IMAGE>

IPC 1-7

**G06F 13/40**; **G06F 13/24**; **G06F 13/36**; **G06F 11/00**

IPC 8 full level

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CPC (source: EP US)

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Cited by

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