

Title (en)

LOW VOLTAGE SHORT CHANNEL TRENCH DMOS TRANSISTOR

Title (de)

NIEDERSPANNUNGS-KURZKANAL-GRABEN-DMOS-TRANSISTOR

Title (fr)

TRANSISTOR MOS A DOUBLE DIFFUSION EN TRANCHEES A CANAL COURT BASSE TENSION

Publication

EP 0853818 A4 19981111 (EN)

Application

EP 96927387 A 19960815

Priority

- US 9613039 W 19960815
- US 53715695 A 19950821

Abstract (en)

[origin: WO9707548A1] A low voltage trench DMOS transistor has simplified punch-through elimination, improved safe operating area and threshold control. The DMOS transistor includes (for an N-channel device), from the top side down, an N+ source region (30), a P-body region (26), a P-drift region (22) and an N+ drain region (20). The trench (38) penetrates down into the drain region (20), with the gate electrode located in the trench (38). When the transistor is reverse-biased, the depletion region spreads from the drain region into the P-drift region (22). The thickness of the drift region determines the drain-source breakdown voltage. Diffusing the body region into the drift region (22) allows control of both the surface concentration in the channel region and the channel length, resulting in improved threshold control. Thus this device has a short channel and a low threshold voltage. A complement P-channel device has similar advantages.

IPC 1-7

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IPC 8 full level

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CPC (source: EP)

H01L 29/1095 (2013.01); **H01L 29/7827** (2013.01); **H01L 29/42368** (2013.01)

Citation (search report)

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- See references of WO 9707548A1

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