Title (en)

Method of manufacturing a bonding substrate

Title (de)

Verfahren zur Herstellung eines verbundenden Substrates

Title (fr)

Procédé de fabrication d'un substrat collé

Publication

EP 0856876 A3 20000726 (EN)

Application

EP 98300615 A 19980128

Priority

JP 3279097 A 19970131

Abstract (en)

[origin: EP0856876A2] A method of manufacturing a bonding substrate is disclosed. An oxide film is formed on the surface of at least one of two semiconductor substrates, and the two substrates are brought into close contact with each other via the oxide film. The substrates are heat-treated in an oxidizing atmosphere in order to firmly join the substrates together. Subsequently, an unjoined portion at the periphery of a device-fabricating substrate is completely removed, and the thickness of the device-fabricating substrate is reduced to a desired thickness so as to yield a thin film. The surface of the thin film is then etched through vapor-phase etching in order to make the thickness of the thin film uniform. In the method, the oxide film on the unjoined portion of at least the support substrate is removed before the surface of the thin film is subjected to vapor-phase etching. The method prevents a groove from being formed in the surface of the unjoined portion (terrace portion) of the support substrate (base wafer) even when the surface of the thin film undergoes vapor phase etching. <IMAGE> <IMAGE>

IPC 1-7

H01L 21/20; H01L 21/304

IPC 8 full level

H01L 21/302 (2006.01); **H01L 21/02** (2006.01); **H01L 21/20** (2006.01); **H01L 21/304** (2006.01); **H01L 27/12** (2006.01)

CPC (source: EP US)

H01L 21/2007 (2013.01 - EP US)

Citation (search report)

- [Y] EP 0547677 A2 19930623 - PHILIPS NV [NL]
- [A] EP 0444942 A1 19910904 - SHINETSU HANDOTAI KK [JP]
- [Y] PATENT ABSTRACTS OF JAPAN vol. 1995, no. 05 30 June 1995 (1995-06-30)
- [A] PATENT ABSTRACTS OF JAPAN vol. 015, no. 269 (E - 1087) 9 July 1991 (1991-07-09)
- [A] PATENT ABSTRACTS OF JAPAN vol. 018, no. 507 (E - 1609) 22 September 1994 (1994-09-22)
- [A] PATENT ABSTRACTS OF JAPAN vol. 1996, no. 08 30 August 1996 (1996-08-30)
- [A] PATENT ABSTRACTS OF JAPAN vol. 1996, no. 04 30 April 1996 (1996-04-30)
- [A] MITANI K ET AL: "Appropriate Wafer Preparation for Thickness Uniformity of PACE-Processed SOI Wafers", PROCEEDINGS OF THE SEVENTH INTERNATIONAL SYMPOSIUM ON SILICON-ON-INSULATOR TECHNOLOGY AND DEVICES, 5 May 1996 (1996-05-05), Los Angeles, CA, USA, pages 87 - 98, XP000913671

Cited by

FR2935535A1; EP1855309A4; FR3024953A1; EP1887612A4; EP2339615A1; FR2954585A1; US9093498B2; US8314007B2; WO2010026006A1; WO2016030610A1

Designated contracting state (EPC)

AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DOCDB simple family (publication)

EP 0856876 A2 19980805; **EP 0856876 A3 20000726**; JP H10223497 A 19980821; US 5918139 A 19990629

DOCDB simple family (application)

EP 98300615 A 19980128; JP 3279097 A 19970131; US 1441598 A 19980127