Title (en)

HIGH CAPACITY ATM SWITCH

Title (de)

ATM-VERMITTLUNG MIT HOHER LEISTUNG

Title (fr)

COMMUTATEUR ATM A HAUT RENDEMENT

Publication

EP 0857383 B1 20020313 (EN)

Application

EP 96932408 A 19961009

Priority

- CA 9600673 W 19961009
- US 54871695 A 19951026

Abstract (en)

[origin: WO9716004A1] An ATM switch architecture expandable to multi-terabits/s uses data transfer in a heterogeneous burst of a constant length. It employs rotators connecting stages in a three-stage switch configuration. In one embodiment, the cells are sorted at ingress and a matching process is performed between the first and middle stages. The switch is simple to control and has high performance at both the call and cell levels. It also meets the basic requirements that cells be delivered in the proper order, and that the rate of any individual connection be as high as the inlet-port rate. With a small internal expansion, the switch is non-blocking in the sense that any bit-rate acceptable to both the inlet and outlet ports will be guaranteed a path through the core. This feature is particularly useful in services which may require frequent bit-rate change during the connection time.

IPC 1-7

H04L 12/56

IPC 8 full level

H04L 12/56 (2006.01); **H04Q 3/00** (2006.01)

CPC (source: EP US)

H04L 12/5601 (2013.01 - EP US); **H04L 49/106** (2013.01 - EP US); **H04L 49/1553** (2013.01 - EP US); **H04L 49/3081** (2013.01 - EP US); **H04L 49/455** (2013.01 - EP US); H04L 2012/565 (2013.01 - EP US); H04L 2012/5681 (2013.01 - EP US)

Cited by

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DE FR GB

DOCDB simple family (publication)

WO 9716004 A1 19970501; CA 2233628 A1 19970501; CA 2233628 C 20020305; DE 69619843 D1 20020418; DE 69619843 T2 20021128; EP 0857383 A1 19980812; EP 0857383 B1 20020313; JP 3074353 B2 20000807; JP H10512422 A 19981124; US 5745486 A 19980428

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