

Title (en)

Data processing system having an instruction pipeline

Title (de)

Datenverarbeitungssystem mit Befehlspipeline

Title (fr)

Système de traitement de données avec pipeline d'instruction

Publication

**EP 0862112 A3 20001206 (EN)**

Application

**EP 98102737 A 19980217**

Priority

- JP 4406497 A 19970227
- JP 28999497 A 19971022

Abstract (en)

[origin: EP0862112A2] A data processing system having a pipeline is provided which includes a CPU designed to fetch a plurality of instructions simultaneously from a memory through a data bus in an instruction fetching stage. Each of the instructions is expressed in a string of bits having a bit length which is shorter than a bus width of the data bus. The instruction fetching stage is effected every instruction processing cycles of a number equal to the number of the instructions simultaneously fetched from the memory for a period of time during which instruction decoding stages of a number equal to the number of simultaneously fetched instructions are effected in the instruction processing cycles in succession. This enables high-speed pipelined operations. <IMAGE>

IPC 1-7

**G06F 9/38**

IPC 8 full level

**G06F 9/38** (2006.01)

CPC (source: EP)

**G06F 9/3802** (2013.01); **G06F 9/3824** (2013.01); **G06F 9/3836** (2013.01); **G06F 9/3869** (2013.01); **G06F 9/3875** (2013.01)

Citation (search report)

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- [A] MCGEADY S: "THE I960CA SUPER SCALAR IMPLEMENTATION OF THE 80960 ARCHITECTURE", WESCON TECHNICAL PAPERS,US,WESTERN PERIODICALS CO. NORTH HOLLYWOOD, VOL. 33, PAGE(S) 628-637, XP000116074
- [A] MELEAR C: "THE DESIGN OF THE 88000 RISC FAMILY", IEEE MICRO,US,IEEE INC. NEW YORK, vol. 9, no. 2, 1 April 1989 (1989-04-01), pages 26 - 38, XP000124913, ISSN: 0272-1732
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Designated contracting state (EPC)

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DOCDB simple family (publication)

**EP 0862112 A2 19980902**; **EP 0862112 A3 20001206**; **EP 0862112 B1 20050921**; DE 69831622 D1 20051027; DE 69831622 T2 20060622; JP 3211750 B2 20010925; JP H10301776 A 19981113

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