

Title (en)

Low current programming of floating gate memory

Title (de)

Schwachstromprogrammieren von schwebenden Gatterspeichern

Title (fr)

Programmation à courant faible de mémoire à porte flottante

Publication

EP 0863514 A2 19980909 (EN)

Application

EP 98301649 A 19980305

Priority

US 81261597 A 19970306

Abstract (en)

A system for programming arrays of floating gate memory cells is provided that reduces programming current requirements, and reduces wordline and bitline stress during programming. A word-to-be-programmed into a floating gate memory array is divided into a plurality of smaller subwords. Only one subword is programmed at a time, thereby reducing programming current requirements. Additionally, subwords which are successfully programmed are not reprogrammed even if bits in other subwords do not program properly. This creates less wordline stress than previous systems which program an entire word at once, thereby requiring subwords which program successfully to be reprogrammed along with subwords which fail to program. Finally, within each subword only those bits which failed to program are reprogrammed, thereby reducing bitline stress during reprogramming for those bits which were successfully programmed.

IPC 1-7

G11C 16/06

IPC 8 full level

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CPC (source: EP US)

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Designated contracting state (EPC)

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