

Title (en)
HIGH VOLTAGE LEVEL SHIFTING CMOS BUFFER

Title (de)
CMOS-PEGELSCHIEBEPUFFER FÜR HOHE SPANNUNGEN

Title (fr)
TAMPON CMOS DE COMMUTATION DE NIVEAU DE HAUTE TENSION

Publication
EP 0864203 A4 20010207 (EN)

Application
EP 97943473 A 19970925

Priority
• US 9716922 W 19970925
• US 72392596 A 19961001

Abstract (en)
[origin: WO9815060A1] A voltage level shifting complementary metal-oxide-silicon (CMOS) buffer (30-47) is arranged and configured to operate in two distinct modes - one of which is high voltage and the other low voltage - depending on the level of the supply voltage (40) to the buffer relative to the operating voltage (VDD) of a device in which the buffer is integrated. In the high voltage mode, in which the supply voltage level exceeds the operating voltage level, the buffer is constrained to perform as a high voltage level shifter. In the low voltage mode, in which the supply voltage level is equal to or less than the operating voltage level, the buffer is constrained to perform as a CMOS logic gate.

IPC 1-7
H03K 19/185; **H03K 19/0948**; **H03K 3/356**; **H03K 17/10**

IPC 8 full level
G11C 16/06 (2006.01); **H03K 3/356** (2006.01); **H03K 17/10** (2006.01); **H03K 19/0185** (2006.01)

CPC (source: EP KR)
H03K 3/356113 (2013.01 - EP KR); **H03K 17/102** (2013.01 - EP KR); **H03K 19/018521** (2013.01 - KR)

Citation (search report)
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• [A] US 5175512 A 19921229 - SELF PAUL W [US]
• [A] WO 9519658 A1 19950720 - F P D TECHNOLOGY INC [US]
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• [X] PATENT ABSTRACTS OF JAPAN vol. 1996, no. 06 28 June 1996 (1996-06-28) & US 5825205 A 19981020 - OHTSUKA NOBUAKI [US]
• See references of WO 9815060A1

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Designated contracting state (EPC)
CH DE ES FR GB IT LI NL SE

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DOCDB simple family (application)
US 9716922 W 19970925; EP 97943473 A 19970925; JP 51661698 A 19970925; KR 19980704021 A 19980529; TW 86114170 A 19970930