

Title (en)

MOS-gated semiconductor devices

Title (de)

Halbleiteranordnungen mit MOS-Gatter

Title (fr)

Dispositifs à semiconducteurs à porte MOS

Publication

**EP 0865080 B1 20100519 (EN)**

Application

**EP 98104281 A 19980310**

Priority

US 81484297 A 19970311

Abstract (en)

[origin: EP0865080A2] A gate electrode control structure of an MOS-gated semiconductor device includes four doped regions including a first (source) region forming a first P-N junction with an enclosing composite region comprising a second, lightly doped (channel) region wholly enclosing a third heavily doped (body) region partly enclosing the first region, and a fourth (drain) region forming a P-N junction with the third region. The gate electrode control structure is fabricated using known gate electrode self-alignment doping processes but, in the process for forming the third heavily doped region, a spacer layer is provided on the gate electrode for defining a spacing between the third region and the channel region. <IMAGE>

IPC 8 full level

**H01L 21/331** (2006.01); **H01L 29/78** (2006.01); **H01L 21/336** (2006.01); **H01L 29/06** (2006.01); **H01L 29/10** (2006.01); **H01L 29/739** (2006.01)

CPC (source: EP KR US)

**H01L 29/0696** (2013.01 - EP US); **H01L 29/1095** (2013.01 - EP US); **H01L 29/66333** (2013.01 - EP US); **H01L 29/78** (2013.01 - KR); **H01L 29/7802** (2013.01 - EP US)

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DOCDB simple family (publication)

**EP 0865080 A2 19980916**; **EP 0865080 A3 19981028**; **EP 0865080 B1 20100519**; CN 1146970 C 20040421; CN 1198003 A 19981104; DE 69841667 D1 20100701; JP 3971838 B2 20070905; JP H10270680 A 19981009; KR 100505271 B1 20051202; KR 19980080128 A 19981125; TW 385496 B 20000321; US 5877044 A 19990302

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