

Title (en)

MULTI-PORT CACHE MEMORY WITH ADDRESS CONFLICT DETECTION

Title (de)

MEHRANSCHLÜSSIGE CACHESPEICHER MIT ADRESSKONFLIKTERKENNUNG

Title (fr)

MEMOIRE CACHE A ACCES MULTIPLES AVEC DETECTION DE CONFLITS D'ADRESSE

Publication

**EP 0875030 A2 19981104 (EN)**

Application

**EP 97940270 A 19970923**

Priority

- IB 9701146 W 19970923
- US 71960996 A 19960925

Abstract (en)

[origin: WO9813763A2] A multi-port cache memory is disclosed. The multi-port cache operates in a microprocessor system, and includes multiple memory banks and multiple ports for enabling accesses to the banks. Conflict detection circuitry detects simultaneous addressing of a first memory bank through a first port and a second port, and stalls microprocessor operations for a predetermined number of clock cycles in response to the detection of simultaneous addressing. Conflict resolution circuitry allows access to the first bank through the first port during the stall, and allows access through the second port after the stall is complete. Generally, the conflict resolution circuitry allows access through ports that are attempting to access the first memory bank in order of ascending priority during successive clock cycles while the microprocessor is stalled. One or more of the ports attempting to access the first bank may be allowed access before or after the time the microprocessor is stalled. Each bank is single-ported. The banks have non overlapping address spaces, and are addressed so that words within a cache block are distributed among multiple banks.

IPC 1-7

**G06F 12/08**

IPC 8 full level

**G06F 12/08** (2006.01); **G06F 12/0846** (2016.01)

CPC (source: EP KR US)

**G06F 12/08** (2013.01 - KR); **G06F 12/0851** (2013.01 - EP US)

Citation (search report)

See references of WO 9813763A2

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