Title (en)

Power output stage for driving the cells of a plasma panel

Title (de)

Leistungsendstufe zum Antreiben von Zellen einer Plasmaanzeigetafel

Title (fr)

Etage de sortie de puissance pour la commande de cellules d'écran à plasma

Publication

EP 0880124 A1 19981125 (FR)

Application

EP 98410053 A 19980518

Priority

FR 9706498 A 19970522

Abstract (en)

The power output stage (30) includes an input (32) receiving a low voltage input logic signal (IN2) and an output (34) supplying a high voltage control signal (OUT2). An output circuit (36) includes a charge transistor, which receives a high voltage potential(VPP) on a drain and has a source connected to an output (34). The output circuit also has a discharge transistor (40) which receives a reference potential (GND) on a source and has a drain connected to the output (34). A control circuit (42,44,46,52,58) supplies control signals (PCDE,NCDE) to the charge and discharge transistors as a function of the input logic signal. The charge and discharge transistors are of the n-channel VDMOS type. The charge transistor (38) is arranged to form a transistor of composite type P. The control circuit is arranged so that the potential at the grid of the charge transistor falls faster than the potential at the output when the input logic signal controls a discharge of the output .

Abstract (fr)

L'invention concerne un étage de sortie de puissance (30) pour la commande de cellules d'écran à plasma. Il comprend deux transistors de charge et de décharge (38, 40) de type VDMOS à canal N, le transistor de charge étant agencé de sorte à former un transistor de type P composite. Ces transistors permettent de fournir un courant de charge à une sortie (34) et d'absorber un courant de décharge provenant de cette sortie. Deux inverseurs (46, 52) sont dimensionnés de sorte que le potentiel de la grille de commande du transistor de charge (38) chute plus rapidement que le potentiel de la sortie lorsque l'on commande une décharge de cette sortie. On réalise, ainsi, un étage de sortie d'encombrement limité et sans risque de conduction simultanée des transistors de charge et de décharge. <IMAGE>

IPC 1-7

G09G 3/28

IPC 8 full level

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CPC (source: EP US)

G09G 3/26 (2013.01 - EP US); **G09G 3/296** (2013.01 - EP US)

Citation (search report)

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