

Title (en)
SUPERSCALAR MICROPROCESSOR INCLUDING A HIGH PERFORMANCE INSTRUCTION ALIGNMENT UNIT

Title (de)
SUPERSKALARER MIKROPROZESSOR MIT HOCHLEISTUNGSEINHEIT ZUR BEFEHLSAUSRICHTUNG

Title (fr)
MICROPROCESSEUR SUPERSCALAIRE COMPORTANT UNE UNITE D'ALIGNEMENT DES INSTRUCTIONS A HAUTES PERFORMANCES

Publication
EP 0896700 A1 19990217 (EN)

Application
EP 96915461 A 19960501

Priority
US 9606164 W 19960501

Abstract (en)
[origin: WO9741509A1] A high performance superscalar microprocessor including an instruction alignment unit is provided which is capable of routing variable byte-length instructions simultaneously to a plurality of decode units which form fixed issue positions within the superscalar microprocessor. The instruction alignment unit may be implemented with a relatively small number of cascaded levels of logic gates, thus accomodating very high frequencies of operation. In one embodiment, the superscalar microprocessor includes an instruction cache for storing a plurality of variable byte-length instructions and a predecode unit for generating predecode tags which identify the location of the start byte of each variable byte-length instruction. An instruction alignment unit is configured to channel a plurality of the variable byte-length instructions simultaneously to predetermined issue positions depending upon the locations of their corresponding start bytes in a cache line. The issue position or positions to which an instruction may be dispatched is limited depending upon the position of the instruction's start byte within a line. By limiting the number of issue positions to which a given instruction within a line may be dispatched, the number of cascaded levels of logic required to implement the instruction alignment unit may be advantageously reduced.

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Citation (search report)
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