Title (en)

SLAVE DSP REBOOTS STALLED MASTER CPU

Title (de)

URLADUNG VON BLOCKIERTEM MUSTER-CPU DURCH EINEN SLAVE-DIGITALSIGNALPROZESSOR

Title (fr)

REINITIALISATION D'UC MAITRESSE BLOQUEE PAR UN PROCESSEUR DE SIGNAL NUMERIQUE ASSERVI

Publication

EP 0920661 A1 19990609 (EN)

Application

EP 98905551 A 19980312

Priority

- IB 9800332 W 19980312
- US 88038797 A 19970623

Abstract (en)

[origin: WO9859288A1] A digital home entertainment system comprises one or more slave processors, e.g, DSPs, for processing specific tasks, and a master processor, e.g., a CPU, for control of the system. The slave processor is capable of rebooting the master processor if the master processor has stalled. This slave-controlled rebooting avoids manual cold rebooting of the system and is particularly advantageous in open-architecture multimedia systems with asynchronously cooperating components.

IPC 1-7

G06F 1/24; H04L 29/14; G06F 15/16

IPC 8 full level

G06F 15/177 (2006.01); **G06F 1/24** (2006.01); **G06F 15/16** (2006.01)

CPC (source: EP KR)

G06F 1/24 (2013.01 - EP KR)

Citation (search report)

See references of WO 9859288A1

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

WO 9859288 A1 19981230; EP 0920661 A1 19990609; JP 2000516745 A 20001212; KR 100518478 B1 20051005; KR 20000068286 A 20001125

DOCDB simple family (application)

IB 9800332 W 19980312; EP 98905551 A 19980312; JP 52932798 A 19980312; KR 19997001430 A 19990222