

Title (en)

PROCESS AND DEVICE FOR OPTIMIZING THE POWER-DOWN CYCLE OF A NON-ENGAGING, INTERRUPTABLE POWER SEMICONDUCTOR SWITCH

Title (de)

VERFAHREN UND VORRICHTUNG ZUR OPTIMIERUNG DES ABSCHALTVORGANGS EINES NICHT EINRASTENDEN, ABSCHALTbaren LEISTUNGS-HALBLEITERSCHALTERS

Title (fr)

PROCEDE ET DISPOSITIF POUR OPTIMISER LE PROCESSUS D'INTERRUPTION D'UN SECTIONNEUR DE PUISSANCE A SEMI-CONDUCTEUR BLOCABLE NON VERROUILLANT

Publication

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Application

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Abstract (en)

[origin: DE19634612A1] This invention concerns a process for optimizing the power-down cycle of a non-engaging, interruptable power semiconductor switch (2) in a saturating power converter and a device for carrying out the process. According to the invention, when the interrupt signal (Saus) arrives, the gate emitter voltage (UGE) of this power-semiconductor switch (2) lowered with the help of a maximally permissible discharge current and its collector-emitter voltage (UCE) are monitored against exceeding a reference voltage (UCEref), the value of which is set so that the collector current (IC) begins to commute, and upon reaching the reference value (UCEref), the discharge current is reduced to a value which is below the value of the maximum permissible discharge current. Thus, the power-down cycle of a non-engaging, interruptable power semiconductor switch (2) is largely optimized, so that the voltage rise and current drop times can be separately controlled.

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