Title (en)

A method of manufacturing an integrated circuit using chemical mechanical polishing and a chemical mechanical polishing system

Title (de)

Chemisch-mechanisches Polierverfahren und System für die Herstellung eines integrierten Schaltkreises

Title (fr)

Système et procédé de polissage mécano-chimique pour la fabrication d'un circuit intégré

Publication

EP 0923122 A3 19991229 (EN)

Application

EP 98309597 A 19981124

Priority

- US 98210997 A 19971201
- US 98094397 A 19971201

Abstract (en)

[origin: EP0923122A2] A method of manufacturing integrated circuits using a carrier fixture. The carrier fixture does not include transport channels or openings for directing a slurry to a substrate being polished and, as a result, damage to the substrate is reduced because the edges adjacent to the substrate are eliminated. The present invention further provides a carrier fixture having an inner support (e.g., 130) coupled to a ring member (e.g., 120) that contacts a substrate (e.g., 200) during the CMP process. The present invention also provides a carrier fixture having inner (e.g., 130) and outer supports (e.g., 125) coupled to a ring member (e.g., 120). <IMAGE>

IPC 1-7

H01L 21/68

IPC 8 full level

B24B 37/04 (2012.01); **H01L 21/304** (2006.01)

CPC (source: EP KR)

B24B 37/042 (2013.01 - EP); **B24B 37/32** (2013.01 - EP); **H01L 21/77** (2013.01 - KR)

Citation (search report)

- [XA] GB 2312181 A 19971022 - SPEEDFAM CORP [US]
- [X] PATENT ABSTRACTS OF JAPAN vol. 013, no. 090 (M - 803) 2 March 1989 (1989-03-02)

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