

Title (en)
A programmable divider circuit

Title (de)
Programmierbare Teilerschaltung

Title (fr)
Circuit diviseur programmable

Publication
EP 0926834 B1 20020320 (EN)

Application
EP 98310160 A 19981211

Priority
GB 9727245 A 19971223

Abstract (en)
[origin: EP0926834A1] A programmable dividing circuit comprises a first plurality N of similar transistor stages (B1,B2) connected in a divide-by-N sequence, where N is an odd integer, the transistor stages being configured so that when the output of the last stage is supplied to the first stage in the sequence, the dividing circuit operates as a divide-by-N circuit in which an output signal is generated which has one cycle for every N cycles of a clock signal applied to the transistor stages, a tri-state inverter (T) selectively connectable in a divide-by-M sequence with a second plurality M of transistor stages (B1,B3,B4), where M is an even integer, and wherein the second plurality includes at least some of said first plurality of transistor stages, including said first stage, whereby when the output of the last stage in the divide-by-M sequence is supplied to the first stage, the circuit operates as a divide-by-M circuit in which an output signal is generated which has one cycle for every M cycles of a clock signal applied to the transistor stages, and a switching circuit (MUX) having at least two inputs and arranged to selectively connect to the first stage the output of the last stage in either the divide-by-N sequence or the divide-by-M sequence whereby the circuit can be programmed to operate as a divide-by-N or divide-by-M circuit.

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IPC 8 full level
H03K 23/54 (2006.01); **H03K 23/66** (2006.01)

CPC (source: EP US)
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Cited by
WO0229973A3; US6518805B2; US6661261B2; US6882189B2; US7005898B2

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