Title (en)

GATE-CONTROLLED THYRISTOR

Title (de)

GATE-GESTEUERTER THYRISTOR

Title (fr)

THYRISTOR A COMMANDE PAR GACHETTE

Publication

EP 0931352 A1 19990728 (DE)

Application

EP 98945056 A 19980729

Priority

- DE 9802154 W 19980729
- DE 19732912 A 19970730
- DE 19739498 A 19970909

Abstract (en)

[origin: US6313485B1] A gate-controlled thyristor in which an IGBT in a first cell and a thyristor in a main cell are connected together in ouch a way that the first cell and the main cell form a lateral FET with a channel of a first conducting type. In an emitter zone of the thyristor, there is a layer embedded that increases the charge carrier recombination in order to reduce the start-up resistance of the gate-controlled thyristor. Trenches, filled with insulated gate electrodes, can be introduced into the lateral FET, so that the FET is a side wall FET.

IPC 1-7

H01L 29/74

IPC 8 full level

H01L 29/74 (2006.01); **H01L 29/749** (2006.01)

CPC (source: EP US)

H01L 29/742 (2013.01 - EP US); **H01L 29/749** (2013.01 - EP US)

Citation (search report)

See references of WO 9907020A1

Designated contracting state (EPC)

DE FR GB IE IT

DOCDB simple family (publication)

US 6313485 B1 20011106; EP 0931352 A1 19990728; JP 2001501383 A 20010130; WO 9907020 A1 19990211

DOCDB simple family (application)

US 28169099 A 19990330; DE 9802154 W 19980729; EP 98945056 A 19980729; JP 51039299 A 19980729