

Title (en)

THRESHOLD ADJUST IN VERTICAL DMOS TRANSISTOR

Title (de)

SCHWELLANPASSUNG IN VERTIKALEM DMOS-TRANSISTOR

Title (fr)

AJUSTEMENT DU SEUIL DANS UN TRANSISTOR DMOS VERTICAL

Publication

EP 0931353 A1 19990728 (EN)

Application

EP 97909973 A 19971016

Priority

- US 9717929 W 19971016
- US 73590996 A 19961025

Abstract (en)

[origin: WO9819344A1] A thick oxide region (64) is provided on an epitaxial layer (54) in turn overlying a semiconductor substrate (50). Base regions are provided on either side of the thick oxide region, and source regions are provided in the respective base regions. After formation of gate oxide portions and a gate, which gate extends over the gate oxide portions and thick oxide region, a threshold adjust implant is undertaken into the channel regions of the device, the thick oxide region blocking ions from reaching the epitaxial layer portion thereunder. In another embodiment, after formation of the gate oxide, gate, sources and drains, a mask portion is provided over a portion of the gate above the epitaxial layer portion between the base regions, so that upon implant of threshold adjust dopant, the mask portion blocks such dopant from reaching the area of the epitaxial layer portion thereunder.

IPC 1-7

H01L 29/76; H01L 21/265

IPC 8 full level

H01L 21/336 (2006.01); **H01L 29/423** (2006.01); **H01L 29/78** (2006.01)

CPC (source: EP US)

H01L 29/42368 (2013.01 - EP); **H01L 29/66712** (2013.01 - EP); **H01L 29/7802** (2013.01 - EP US)

Designated contracting state (EPC)

AT BE DE FR GB IT NL SE

DOCDB simple family (publication)

WO 9819344 A1 19980507; EP 0931353 A1 19990728; EP 0931353 A4 19990811

DOCDB simple family (application)

US 9717929 W 19971016; EP 97909973 A 19971016