

Title (en)
METHOD FOR MANUFACTURING A MEMORY CELL CONFIGURATION

Title (de)
VERFAHREN ZUR HERSTELLUNG EINER SPEICHERZELLENANORDNUNG

Title (fr)
MODE DE FABRICATION D'UNE CONFIGURATION DE CELLULES DE MEMOIRE

Publication
EP 0946981 A1 19991006 (DE)

Application
EP 97947716 A 19971104

Priority
• DE 9702549 W 19971104
• DE 19653107 A 19961219

Abstract (en)
[origin: DE19653107A1] In order to manufacture a memory cell configuration comprising a first series of memory cells including a vertical MOS transistor and a second series of memory cells without MOS transistor, the memory cells being arranged along the opposing flanks of strip-shaped pits, tiled memory cells are built one after the other along said pits (5). The spacing between the memory cells is determined according to a spacer technology enabling to meet the space need per memory cell, i.e. $1F < 2\lambda$, where F represents the minimum structural quantity specific to said technology.

IPC 1-7
H01L 21/8246; **H01L 27/112**

IPC 8 full level
H01L 21/8246 (2006.01); **H01L 27/112** (2006.01)

CPC (source: EP KR US)
H10B 20/00 (2023.02 - EP US); **H10B 99/00** (2023.02 - KR)

Citation (search report)
See references of WO 9827586A1

Cited by
US8375941B2

Designated contracting state (EPC)
DE FR GB IT

DOCDB simple family (publication)
DE 19653107 A1 19980702; **DE 19653107 C2 19981008**; EP 0946981 A1 19991006; JP 2001506408 A 20010515; KR 20000057653 A 20000925; TW 349265 B 19990101; US 6153475 A 20001128; WO 9827586 A1 19980625

DOCDB simple family (application)
DE 19653107 A 19961219; DE 9702549 W 19971104; EP 97947716 A 19971104; JP 52716098 A 19971104; KR 19997005459 A 19990617; TW 86116969 A 19971114; US 33149599 A 19990621