

Title (en)

A method of balancing the load in a process for sorting objects

Title (de)

Eine Methode zum Ausgleichen der Last in einem Prozess zum Sortieren von Gegenständen

Title (fr)

Un procédé d'équilibrage de charge dans un procédé de tri d'objets

Publication

EP 0947962 A3 20000517 (EN)

Application

EP 99105376 A 19990316

Priority

IT TO980233 A 19980317

Abstract (en)

[origin: EP0947962A2] The sorting process comprises performing a first and at least a second consecutive sorting cycle by means of a postal machine and the present invention relates to a method of balancing to be performed before the commencement of the sorting process and comprising the step of performing, in at least one of the sorting cycles, at least one of the following procedures: a) a first procedure of balancing the load of the outputs of the postal machine in the current sorting cycle based on at least one of the following balancing criteria: shifting the delivery addresses from the outputs to which they are assigned to respective logically contiguous outputs associated with the same postman; bisection of delivery address into respective pairs of virtually separate delivery address and allocating them to a respective pair of logically contiguous outputs associated with the same postman; and allocation of further outputs to postmen on the basis of an order of criticality of the outputs already allocated to the postman themselves; and b) a second procedure of balancing the load of the outputs of the postal machine in the current sorting cycle based on at least one of the following balancing criteria: distribution over outputs utilised in the current sorting cycle of delivery addresses allocated to each output at the end of the subsequent sorting cycle; shifting the delivery addresses from the outputs to which they are allocated to respective logically contiguous outputs; exchange of delivery addresses between logically contiguous outputs; and bisection of delivery addresses into respective pairs of virtually separate delivery addresses and allocating them to a respective pair of logically contiguous outputs. <IMAGE>

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Citation (search report)

- [XA] DE 19647973 C1 19970925 - AEC ELECTROCOM GMBH [DE]
- [XA] DE 19625007 A1 19980102 - SIEMENS AG [DE]
- [XA] US 5353938 A 19941011 - LAGRANGE HERV E [FR], et al
- [XA] EP 0718049 A2 19960626 - HITACHI LTD [JP]
- [A] DE 19709232 A1 19971106 - HITACHI LTD [JP]
- [A] US 5363971 A 19941115 - WEEKS HORACE W [US], et al

Cited by

EP1090692A3; CN110648091A; US6576857B1

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