Title (en)

ARRANGEMENT FOR CONTROLLING PARALLEL LINES IN A STORAGE CELL ARRANGEMENT

Title (de)

ANORDNUNG ZUR ANSTEUERUNG PARALLELER LEITUNGEN EINER SPEICHERZELLENANORDNUNG

Title (fr)

AGENCEMENT POUR COMMANDER LES LIGNES PARALLELES D'UN DISPOSITIF A CELLULES DE MEMOIRE

Publication

EP 0951738 A1 19991027 (DE)

Application

EP 97951073 A 19971112

Priority

- DE 9702654 W 19971112
- DE 19652538 A 19961217

Abstract (en)

[origin: WO9827593A1] In order to control parallel lines, for example bit lines (BLn) of a storage cell arrangement with doped regions in a semiconductor substrate, several lines (BLn) are electrically connected to one another and to a common node (K). Several selection lines (ALn) are provided transversely to the lines (BLn). At their crossing points are arranged MOS-transistors (M1, M2) mounted in series along one of the lines (BLn) and whose gate electrodes are formed by the corresponding selection line (ALn). At least one MOS-transistor (M1) in each of the parallel lines (BL1) has a higher operation voltage than the others.

IPC 1-7

H01L 27/112

IPC 8 full level

G11C 5/02 (2006.01); **H10B 20/00** (2023.01)

CPC (source: EP KR US)

H01L 27/0207 (2013.01 - EP US); **H01L 27/11803** (2013.01 - EP US); **H10B 20/00** (2023.02 - KR); **H10B 20/383** (2023.02 - EP US); **H10B 20/65** (2023.02 - EP US)

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

WO 9827593 A1 19980625; EP 0951738 A1 19991027; JP 2001506409 A 20010515; KR 100408575 B1 20031206; KR 20000057660 A 20000925; TW 363266 B 19990701; US 6125050 A 20000926

DOCDB simple family (application)

DE 9702654 W 19971112; EP 97951073 A 19971112; JP 52716698 A 19971112; KR 19997005480 A 19990617; TW 86117354 A 19971120; US 33536599 A 19990617