Title (en)

Method of providing clock signals to load circuits in an ASIC device

Title (de)

Verfahren zur Versorgung von Lastkreisen mit Taktsignalen in einer ASIC-Vorrichtung

Title (fr)

Procédé pour la distribution de signaux d'horloge à des circuits de charge dans un dispositif ASIC

Publication

EP 0953892 A1 19991103 (EN)

Application

EP 98107883 A 19980429

Priority

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Abstract (en)

A method of providing clock signals to load circuits in a ASIC device having a balanced clock tree including a master clock line, for e.g. a clock trunk or H-tree, and branched clock lines feeding the clock signals to load circuits and being balanced with respect to the delays and loads in domains of the ASIC device to which the branched clock lines supply clock signals, is characterized by generating derived clock signals by gating the master clock signal which derived clock signals have a frequency reduced by a factor n > 1 (n=2,...,N) adapted to the need of the load circuits in a particular domain, and routing the master clock signal and/or derived clock signal for a particular domain to the load circuit of said domain. An ASIC device has gating circuits for generating derived clock signals and means for routing the master clock signal and/or derived clock signal for a partiular domain to the load circuits of said domain. Furthermore, a method of providing clock signals to load circuits in a ASIC device having a plurality of balanced clock tree systems each including a master clock line, for example a clock trunk or H-tree system, and branched clock lines feeding the clock signals to load circuits and being balanced with respect to the delays and loads in domains of the ASIC device to which the branched clock lines supply clock signals, is also characterized by multiplexing the master clock signal of a clock system or a test clock signal into the clock system by controlling the muliplexing operation by test enable signal and inverted test enable signal whereby the master clock signal or the test clock signal is supplied to the clock system. Another ASIC device comprise multiplexer units for muliplexing the master clock signal of a clock system or a test clock signal into the clock system, said multiplexer units being controlled by a test enable signal and an inverted test enable signal whereby the master clock signal or the test clock signal is supplied to the clock system. <IMAGE>

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IPC 8 full level

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CPC (source: EP US)

G01R 31/30 (2013.01 - EP US); **G06F 1/06** (2013.01 - EP US); **G06F 1/10** (2013.01 - EP US)

Citation (search report)

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Designated contracting state (EPC)

DE

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