Title (en)

Detecting communication errors across a chip boundary

Title (de)

Kommunikationsfehlererkennung an einem Chipübergang

Title (fr)

Détection des erreurs de communication aux limites d'une puce

Publication

EP 0957429 B1 20030122 (EN)

Application

EP 98309735 A 19981127

Priority

GB 9810512 A 19980515

Abstract (en)

[origin: EP0957429A1] An integrated circuit comprises a connection port having a serial data input pin and a serial data output pin, on-chip functional circuitry and test logic, and a test access port controller connected to effect communication of serial data across the chip boundary via said input and output pins. The test access port controller is connectable to the test logic in a first mode of operation to effect communication of serial test data under control of an incoming clock signal and being operable in a second mode of operation to communication data as a sequence of serial bits according to a predetermined protocol between the connection port and the on-chip functional circuitry. The integrated circuit includes error detection means for detecting an error condition in the protocol and gating circuitry responsive to detection of the error condition to prevent communication of subsequent data until the error condition is detected as having been removed. <IMAGE>

IPC 1-7

G06F 11/00

IPC 8 full level

G01R 31/3185 (2006.01); **G06F 11/00** (2006.01)

CPC (source: EP US)

G01R 31/31855 (2013.01 - EP US); **G06F 11/0763** (2013.01 - EP US)

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0957429 A1 19991117; **EP 0957429 B1 20030122**; DE 69810896 D1 20030227; GB 9810512 D0 19980715; US 6381721 B1 20020430

DOCDB simple family (application)

EP 98309735 A 19981127; DE 69810896 T 19981127; GB 9810512 A 19980515; US 31199099 A 19990514