Title (en)

Calibrated delay locked loop for DDR SDRAM applications

Title (de)

Kalibrierte Verzögerungsregelschleife für DDR-SDRAM-Anwendungen

Title (fr)

Boucle à verrouillage de retard pour applications DDR SDRAM

Publication

EP 0967724 A3 20031015 (EN)

Application

EP 99109998 A 19990521

Priority

US 10387198 A 19980624

Abstract (en)

[origin: EP0967724A2] A calibrated Delay Locked Loop (DLL) arrangement synchronizes an output data signal thereof to an input clock signal. A delay line receives the input clock signal and generates a clock output signal having a selective delay. A gating circuit receives the clock output signal and separately generates an imitation data signal that corresponds to the clock output signal, and latches an input data signal with the output clock signal to generate an output data signal. The gating circuit is also responsive to a switching control signal having a first logical value for providing only the output data signal to an output thereof, and to the switching control signal having a second logical value for providing only the imitation data signal to an output thereof. A driver receives the gating circuit output signal and provides this signal as the calibrated DLL arrangement output data signal. A phase comparator in a feedback loop from the output of the driver is responsive to the switching control signal having the second logical value for comparing the input clock signal and the imitation data signal appearing at the driver output, and for causing the delay line to selectively synchronize the imitation data signal to the input clock signal. A switching control signal having the first logical value idles the phase comparator and maintains a latest delay introduced by the delay line.

IPC 1-7

H03L 7/081; G11C 7/00

IPC 8 full level

H04L 7/033 (2006.01); **G11C 7/22** (2006.01); **H03K 5/13** (2006.01); **H03L 7/081** (2006.01)

CPC (source: EP KR US)

G11C 7/1066 (2013.01 - EP US); **G11C 7/22** (2013.01 - EP US); **G11C 7/222** (2013.01 - EP US); **H03K 5/13** (2013.01 - KR); **H03L 7/081** (2013.01 - KR); **H03L 7/0816** (2013.01 - EP US)

Citation (search report)

[A] GB 2316208 A 19980218 - FUJITSU LTD [JP]

Cited by

CN103259702A; US7259634B2; US6834255B2; WO2009067326A1; WO0190864A3; US8208593B2; US8649475B2

Designated contracting state (EPC)

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