

Title (en)
FLATTENING PROCESS FOR BONDED SEMICONDUCTOR SUBSTRATES

Title (de)
PLANARISIERUNGSPROZESS FÜR VERBUNDENE HALBLEITERSUBSTRATE

Title (fr)
PROCEDE D'APLATISSEMENT POUR SUBSTRATS SEMI-CONDUCTEURS LIES

Publication
EP 0968081 A4 20000202 (EN)

Application
EP 97937023 A 19970806

Priority
• US 9713069 W 19970806
• US 71136096 A 19960904

Abstract (en)
[origin: WO9809804A1] Process for the preparation of a substrate having a semiconductor layer of a target thickness, T_t. In the process, two wafers are bonded face to face to form a substrate wherein one of the wafers has a known thickness, T_{known}, and a total thickness variation of less than about 0.75 micrometers and the second wafer comprises a layer of semiconductor material. The substrate is thinned in a first stock removal step to reduce the thickness of the semiconductor layer. The distance between the front and back surfaces of the thinned substrate at discrete positions on said front surface is measured to generate thickness profile data. Additional stock is removed from the front surface of the thinned substrate in a second stock removal step to reduce the thickness of the semiconductor layer to the target thickness, T_t, with the amount of stock being removed at each of said discrete positions being determined after taking into account the thickness profile data, T_t, and T_{known}.

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CPC (source: EP KR)
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Citation (search report)
• [E] EP 0797248 A2 19970924 - SHINETSU HANDOTAI KK [JP]
• [A] US 5413951 A 19950509 - OHORI TATSUYA [JP], et al
• [X] PATENT ABSTRACTS OF JAPAN vol. 1995, no. 5 30 June 1995 (1995-06-30)
• See references of WO 9809804A1

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DOCDB simple family (application)
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