Title (en)

INTEGRATED CIRCUIT AND METHOD FOR TESTING THE SAME

Title (de)

INTEGRIERTE SCHALTUNG UND VERFAHREN ZUM TESTEN DER INTEGRIERTEN SCHALTUNG

Title (fr)

CIRCUIT INTEGRE ET PROCEDE POUR ESSAYER LEDIT CIRCUIT INTEGRE

Publication

EP 0968436 A2 20000105 (DE)

Application

EP 98916822 A 19980302

Priority

- DE 9800608 W 19980302
- DE 19711478 A 19970319

Abstract (en)

[origin: DE19711478A1] The invention relates to an integrated circuit with a CPU and a user ROM characterized by a test ROM whose address range is located inside the user ROM address range, a RAM located outside the CPU and switching means enabling access to either the user ROM or the test ROM and which can be irreversibly placed in a state allowing access to the user ROM only.

IPC 1-7

G01R 31/317

IPC 8 full level

G06F 11/22 (2006.01); **G06F 12/14** (2006.01); **G06F 21/24** (2006.01); **G06K 19/07** (2006.01)

CPC (source: EP KR)

G06F 11/22 (2013.01 - EP KR); **G06K 19/07** (2013.01 - EP)

Citation (search report)

See references of WO 9841880A3

Designated contracting state (EPC)

AT CH DE ES FR GB IT LI

DOCDB simple family (publication)

DE 19711478 A1 19981001; BR 9808381 A 20000523; CN 1251183 A 20000419; EP 0968436 A2 20000105; JP 2001527669 A 20011225; KR 20000076351 A 20001226; WO 9841880 A2 19980924; WO 9841880 A3 19990114

DOCDB simple family (application)

DE 19711478 A 19970319; BR 9808381 A 19980302; CN 98803503 A 19980302; DE 9800608 W 19980302; EP 98916822 A 19980302; JP 54000998 A 19980302; KR 19997008452 A 19990917