Title (en)

Semiconductor integrated circuit memory

Title (de)

Integrierte Halbleiterspeicherschaltung

Title (fr)

Circuit de mémoire intégré à semi-conducteur

Publication

EP 0969476 A1 20000105 (EN)

Application

EP 99305089 A 19990629

Priority

JP 18509798 A 19980630

Abstract (en)

A semiconductor memory includes memory cell blocks (12a - 12d), a burst-length information generating circuit (4) which generates burst-length information (b18) based on a burst length, and a block enable circuit (6) which receives the burst-length information. The block enable circuit selectively enables one of the memory cell blocks when the burst length is equal to or shorter than a predetermined burst length and selectively enables a plurality of memory cell blocks based on the burst length when the burst length is longer than the predetermined burst length. Data are read from the above-mentioned one or plurality of memory cell blocks. <IMAGE>

IPC 1-7

G11C 7/00

IPC 8 full level

G11C 7/00 (2006.01); **G11C 7/10** (2006.01)

CPC (source: EP KR US)

G11C 7/00 (2013.01 - KR); **G11C 7/1018** (2013.01 - EP US); **G11C 7/1072** (2013.01 - EP US)

Citation (search report)

- [A] US 5703828 A 19971230 - PARK CHUROO [KR], et al
- [A] US 5386385 A 19950131 - STEPHENS JR MICHAEL C [US]
- [A] WO 9819248 A1 19980507 - 3COM CORP [US]
- [A] EP 0778575 A2 19970611 - IBM [US]
- [A] US 5657287 A 19970812 - MCLAURY LOREN L [US], et al

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

EP 0969476 A1 20000105; **EP 0969476 B1 20060329**; DE 69930586 D1 20060518; DE 69930586 T2 20060831; KR 100567991 B1 20060406; KR 20000006561 A 20000125; TW 426857 B 20010321; US 6185149 B1 20010206

DOCDB simple family (application)

EP 99305089 A 19990629; DE 69930586 T 19990629; KR 19990025561 A 19990630; TW 88111007 A 19990629; US 34014799 A 19990628