

Title (en)

METHOD FOR DESIGNING COMPLEX, DIGITAL AND INTEGRATED CIRCUITS AND A CIRCUIT STRUCTURE FOR CARRYING OUT SAID METHOD

Title (de)

VERFAHREN ZUM ENTWURF KOMPLEXER, DIGITALER UND INTEGRIERTER SCHALTUNGEN SOWIE SCHALTUNGSSTRUKTUR ZUR DURCHFÜHRUNG DES VERFAHRENS

Title (fr)

PROCEDE POUR LA CONCEPTION DE CIRCUITS NUMERIQUES ET INTEGRES COMPLEXES ET STRUCTURE DE CIRCUIT POUR LA MISE EN OEUVRE DE CE PROCEDE

Publication

EP 0974112 A1 20000126 (DE)

Application

EP 98930641 A 19980408

Priority

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- DE 19714756 A 19970410
- DE 19731043 A 19970719

Abstract (en)

[origin: WO9845794A1] The data flows of a system are allocated an arithmetic or logical function per function block (ALU-block), forming a RAM control. The ALU-blocks are specialised according to individual processing tasks of the data flows. The current status of the RAM address and RAM output data are recoupled with the ALU-blocks. During operation, the ALU-blocks alternately produce write accesses to the RAM and read accesses of all the ALU-blocks can occur with every cycle, thereby controlling the outgoing signal lines of the data flows. Registers are inserted in such a way that the ALU-blocks are placed between register levels to ensure that test patterns are generated automatically with existing CAE programs. The low use of test structures guarantees that the base circuit has good testability with a minimal test pattern rate at an early stage of the circuit design. The inventive circuit structure can also be configured as a digital signal processor.

IPC 1-7

G06F 17/50; G06F 11/267

IPC 8 full level

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CPC (source: EP US)

G01R 31/318591 (2013.01 - EP US); **G06F 7/48** (2013.01 - EP US); **G06F 9/3001** (2013.01 - EP US); **G06F 11/27** (2013.01 - EP US); **G06F 30/30** (2020.01 - EP US); **G06F 30/33** (2020.01 - EP US); **G06F 30/3308** (2020.01 - US)

Citation (search report)

See references of WO 9845794A1

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