

Title (en)
Programmable architecture computer

Title (de)
Computer mit programmierbarer Architektur

Title (fr)
Ordinateur à architecture programmable

Publication
EP 0978792 A1 20000209 (EN)

Application
EP 98830480 A 19980805

Priority
EP 98830480 A 19980805

Abstract (en)
A computer having a control unit (CU) provided with at least one microprogram elaboration unit (EU) which is connected with an input/output control unit (IOU) and with an address formation unit (AF) of at least one main memory (MM), wherein said control unit (CU) is connected in parallel with a plurality of execution modules (XMn), each of which comprises a programmable switch matrix (XSM), to which an internal elaboration unit (XEU), an additional unit for the formation of memory addresses (XAF) and at least one programmable gate matrix (XGn) are connected, respectively.
<IMAGE>

IPC 1-7
G06F 15/78; **G06F 9/38**

IPC 8 full level
G06F 9/38 (2006.01); **G06F 15/78** (2006.01)

CPC (source: EP)
G06F 9/30145 (2013.01); **G06F 9/3897** (2013.01); **G06F 15/7867** (2013.01)

Citation (search report)

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- [A] EP 0825540 A1 19980225 - SIEMENS AG [DE]
- [A] WO 9832071 A2 19980723 - INFINITE TECHNOLOGY CORP [US]
- [A] ISELI C ET AL: "SPYDER: A SURE(SUPERSCALAR AND RECONFIGURABLE) PROCESSOR", JOURNAL OF SUPERCOMPUTING, vol. 9, no. 3, 1 January 1995 (1995-01-01), pages 231 - 252, XP000589467

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DE FI FR GB IT NL SE

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