

Title (en)
Multilayer type chip inductor

Title (de)
Mehrschichtige Chip-Induktivität

Title (fr)
Inductance de puce multicouche

Publication
EP 0978852 A1 20000209 (EN)

Application
EP 99114703 A 19990727

Priority
KR 19980031688 A 19980804

Abstract (en)
A multilayer type chip inductor includes a pair of outermost sheets having a terminal pattern, respectively, wherein the terminal patterns are, respectively, identical in shape, each terminal pattern including a via hole and being capable of providing various positions for the via hole for electrically connecting the terminal pattern to the various conductor patterns of the intermediate sheet. <IMAGE>

IPC 1-7
H01F 27/28; **H01F 17/00**

IPC 8 full level
H01F 27/00 (2006.01); **H01F 17/00** (2006.01); **H01F 27/28** (2006.01)

CPC (source: EP KR)
H01F 17/0006 (2013.01 - EP); **H01F 27/00** (2013.01 - KR); **H01F 27/2804** (2013.01 - EP)

Citation (search report)

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- [A] FR 2379229 A1 19780825 - EUROFARAD [FR]
- [XY] PATENT ABSTRACTS OF JAPAN vol. 1997, no. 07 31 July 1997 (1997-07-31)
- [X] PATENT ABSTRACTS OF JAPAN vol. 018, no. 311 (E - 1561) 14 June 1994 (1994-06-14)
- [A] PATENT ABSTRACTS OF JAPAN vol. 018, no. 573 (E - 1624) 2 November 1994 (1994-11-02)
- [A] PATENT ABSTRACTS OF JAPAN vol. 018, no. 599 (E - 1631) 15 November 1994 (1994-11-15)
- [A] PATENT ABSTRACTS OF JAPAN vol. 1997, no. 11 28 November 1997 (1997-11-28)
- [A] PATENT ABSTRACTS OF JAPAN vol. 018, no. 311 (E - 1561) 14 June 1994 (1994-06-14)

Designated contracting state (EPC)
DE FR GB

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