Title (en)

Combined precharge and equalisation circuit

Title (de)

Kombinierte Vorlade- und Homogenisierschaltung

Title (fr)

Circuit de précharge et d'égalisation

Publication

EP 0980074 B1 20050615 (DE)

Application

EP 99115517 A 19990805

Priority

DE 19836736 A 19980813

Abstract (en)

[origin: DE19836736C1] Combined precharging- and homogenisation circuit includes first and second FET type precharging transistors (1,3) and a homogenisation (equalising) transistor (2) connected in series between the two precharging transistors. The common gate (11,12) arrangement is an angled structure turned through approx. 45 deg. relative to the bit lines length (BLT,BLC). The common drain (7,10) and the common source/drain (8,9) are brought out over the common gate (11,12) and have zones jutting out, with the bit line contacts (15) located in these salient zones.

IPC 1-7

G11C 7/12

IPC 8 full level

G11C 7/12 (2006.01); **H10B 12/00** (2023.01)

CPC (source: EP KR US)

G11C 7/12 (2013.01 - EP US); **G11C 11/40** (2013.01 - KR); **H10B 12/00** (2023.02 - EP US)

Designated contracting state (EPC)

DE FR GB IE IT

DOCDB simple family (publication)

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