Title (en)

PROCESSOR INTERFACING TO MEMORY MAPPED COMPUTING ENGINE

Title (de)

PROZESSOR, DER MIT EINER SPEICHERABBILDENDEN RECHENMACHINE EINE SCHNITTSTELLE BILDET

Title (fr)

PROCESSEUR ASSURANT L'INTERFACE A UN MOTEUR DE CALCUL MEMO-CENTRIQUE

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Application

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Abstract (en)

[origin: WO9855932A2] A memory subsystem that is partitioned into two or more blocks of memory space in which one block of the memory communicates with an I/O or DMA channel to load data, while the other block of memory simultaneously communicates with one or more execution units that carry out arithmetic operations on data in the second block. Results are written back to the second block of memory. Upon conclusion of that process, the memory blocks are effectively "swapped" so that the second block, now holding processed (output) data, communicates with the I/O channel to output that data, while the execution unit communicates with the first block, which by then has been filled with new input data. Methods and apparatus are shown for implementing this memory swapping technique in real time so that the execution unit is never idle. A method of interfacing a processor bus to a computation engine having a microprogrammable memory-centric controller and an array of memory, comprising the steps of providing a predetermined series of microcode instructions for execution by the MCC; selecting a start address within the series of microcode instructions for carrying out a corresponding operation; and executing the series of microcode instructions in the MCC beginning at the selected start address so as to carry out the corresponding operation in the engine. The present invention is useful in a wide variety of signal processing applications including programmable MPEG encode and decode, graphics, speech processing, image processing, array processors, etc. In telecommunications, the invention can be used, for example, for switching applications in which multiple I/O channels are operated simultaneously.

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