Title (en)

Digital signal processor

Title (de)

Digitaler Signalprozessor

Title (fr)

Processeur de signaux numériques

Publication

EP 0992916 A1 20000412 (EN)

Application

EP 98402455 A 19981006

Priority

EP 98402455 A 19981006

Abstract (en)

A processor (100) is provided that is a programmable fixed point digital signal processor (DSP) with variable instruction length, offering both high code density and easy programming. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks, The processor includes an instruction buffer unit (106), a program flow control unit (108), an address/data flow unit (110), a data computation unit (112), and multiple interconnecting busses. Dual multiply-accumulate blocks improve processing performance. A memory interface unit (104) provides parallel access to data and instruction memories. The instruction buffer is operable to buffer single and compound instructions pending execution thereof. A decode mechanism is configured to decode instructions from the instruction buffer. The use of compound instructions enables effective use of the bandwidth available within the processor. A soft dual memory instruction can be compiled from separate first and second programmed memory instructions. Instructions can be conditionally executed or repeatedly executed. Bit field processing and various addressing modes, such as circular buffer addressing, further support execution of DSP algorithms. The processor includes a multistage execution pipeline with pipeline protection features. Various functional modules can be separately powered down to conserve power. The processor includes emulation and code debugging facilities with support for cache analysis. <IMAGE>

IPC 1-7 (main, further and additional classification)

G06F 15/78; G06F 9/38

IPC 8 full level (invention and additional information)

G06F 5/01 (2006.01); **G06F 7/60** (2006.01); **G06F 7/74** (2006.01); **G06F 7/76** (2006.01); **G06F 9/30** (2006.01); **G06F 9/308** (2006.01); **G06F 9/315** (2006.01); **G06F 9/318** (2006.01); **G06F 9/32** (2006.01); **G06F 9/355** (2006.01); **G06F 9/38** (2006.01); H04M 1/73 (2006.01)

CPC (invention and additional information)

G06F 7/764 (2013.01); **G06F 5/01** (2013.01); **G06F 7/607** (2013.01); **G06F 7/74** (2013.01); **G06F 7/762** (2013.01); **G06F 9/30014** (2013.01); **G06F 9/30018** (2013.01); **G06F 9/30032** (2013.01); **G06F 9/30043** (2013.01); **G06F 9/30083** (2013.01); **G06F 9/3013** (2013.01); **G06F 9/30149** (2013.01); **G06F 9/30181** (2013.01); **G06F 9/30189** (2013.01); **G06F 9/32** (2013.01); **G06F 9/321** (2013.01); **G06F 9/325** (2013.01); **G06F 9/3552** (2013.01); **G06F 9/3836** (2013.01); **G06F 9/3838** (2013.01); **G06F 9/384** (2013.01); **G06F 9/3855** (2013.01); **G06F 9/3867** (2013.01); **G06F 9/3879** (2013.01); **G06F 9/3885** (2013.01); **G06F 9/3891** (2013.01); **G06K 13/0825** (2013.01)

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