

Title (en)  
DUAL DAMASCENE ETCH PROCESS

Title (de)  
ZWEIFACHES DAMASZENER-ÄTZVERFAHREN

Title (fr)  
PROCEDE DE GRAVURE A DOUBLE DAMASQUINAGE

Publication  
**EP 0995228 A1 20000426 (EN)**

Application  
**EP 98915322 A 19980407**

Priority  
• US 9806828 W 19980407  
• US 88319797 A 19970626

Abstract (en)  
[origin: WO9900839A1] A semiconductor process in which a semiconductor substrate (104) including a first interconnect level (108) is provided. An interlevel dielectric layer (110) is formed on the semiconductor substrate and a contact masking layer (122) is formed on the interlevel dielectric (110). A pattern of the contact masking layer (122) is aligned over a contact region (112) of the interlevel dielectric (110). An interconnect masking (130) layer is then formed on the contact masking layer (122). A pattern of the interconnect masking layer (130) is aligned over an interconnect region (136) of the interlevel dielectric layer (110). Portions of the contact region (112) are then selectively removed to form a contact tunnel (140). Portions of the interconnect region (136) are then selectively removed to form an interconnect trench (150). The contact tunnel (140) and the interconnect trench (150) are then filled with a conductive material (160). In the preferred embodiment, the contact masking layer (122) comprises a silicon nitride layer. The interconnect masking layer (130) is preferably a patterned photoresist layer formed on the contact masking layer (122). The formation of the interconnect masking layer (130) preferably precedes the step of selectively removing portions of the contact region (112) such that the interconnect masking layer (130) and the contact masking layer (122) are simultaneously present upon the interlevel dielectric layer (110) prior to the formation of the contact tunnels (140). In one embodiment, the filling of the contact tunnel and the filling of the interconnect trench are accomplished simultaneously. Ideally, selective removal of portions of the interconnect region vertically translates the contact tunnel within the interlevel dielectric such that the contact tunnel extends to an upper surface of the first interconnect level.

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