

Title (en)
TRANSLATED MEMORY PROTECTION APPARATUS FOR AN ADVANCED MICROPROCESSOR

Title (de)
SPEICHERSCHUTZEINRICHTUNG ZUM SCHUTZ GEGEN ÜBERSETZTE BEFEHLE FÜR EINEN MIKROPROZESSOR

Title (fr)
DISPOSITIF DE PROTECTION DE MEMOIRE D'INSTRUCTIONS TRADUITES POUR MICROPROCESSEUR EVOLUE

Publication
EP 1004075 A4 20010117 (EN)

Application
EP 97939380 A 19970811

Priority
US 9714117 W 19970811

Abstract (en)
[origin: WO9908191A1] A method of responding to an attempt to write a memory address including a target instruction which has been translated to a host instruction for execution by a host processor including the steps of marking a memory address including a target instruction which has been translated to a host instruction, detecting a memory address which has been marked when an attempt is made to write to the memory address, and responding to the detection of a memory address which has been marked by protecting a target instruction at the memory address until it has been assured that translations associated with the memory address will not be utilized before being updated.

IPC 1-7
G06F 9/455; G06F 12/00; G06F 12/14; G06F 12/16; G06F 13/00

IPC 8 full level
G06F 9/30 (2006.01); **G06F 9/318** (2006.01); **G06F 9/38** (2006.01); **G06F 9/455** (2006.01); **G06F 12/10** (2006.01); **G06F 12/14** (2006.01)

CPC (source: EP KR)
G06F 9/3812 (2013.01 - EP); **G06F 9/45504** (2013.01 - EP); **G06F 12/14** (2013.01 - KR); **G06F 12/145** (2013.01 - EP)

Citation (search report)
• [XA] KEMAL EBCIOGLU, ERIK R. ALTMAN: "DAISY: Dynamic Compilation for 100% Architecture Compatibility", INTERNET DOCUMENT: IBM RESEARCH REPORT, 8 May 1996 (1996-05-08), XP002152424, Retrieved from the Internet <URL:[http://domino.watson.ibm.com/library/cyberdig.nsf/a3807c5b4823c53f85256561006324be/fd183b4dacc05b7585256593007209e7/\\$FILE/8502.ps.gz](http://domino.watson.ibm.com/library/cyberdig.nsf/a3807c5b4823c53f85256561006324be/fd183b4dacc05b7585256593007209e7/$FILE/8502.ps.gz)> [retrieved on 20001107]
• [XA] GABRIEL M. SILBERMAN, KEMAL EBCIOGLU: "AN ARCHITECTURAL FRAMEWORK FOR MIGRATION FROM CISC TO HIGHER PERFORMANCE PLATFORMS", INTERNATIONAL CONFERENCE ON SUPERCOMPUTING, CONFERENCE PROCEEDINGS, 19 July 1992 (1992-07-19), XP000576925
• [A] MANOJ FRANKLIN, MARK SMOTHERMAN: "A FILL-UNIT APPROACH TO MULTIPLE INSTRUCTION ISSUE", PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE, November 1994 (1994-11-01), XP000874608
• See references of WO 9908191A1

Designated contracting state (EPC)
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WO 9908191 A1 19990218; CA 2283560 A1 19990218; CA 2283560 C 20031209; EP 1004075 A1 20000531; EP 1004075 A4 20010117;
JP 2001519955 A 20011023; JP 3621116 B2 20050216; KR 100421687 B1 20040310; KR 20010014096 A 20010226

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