

Title (en)  
FAULT-TOLERANT ARCHITECTURE FOR IN-CIRCUIT PROGRAMMING

Title (de)  
FEHLERTOLERANTE ARCHITEKTUR FÜR IN-CIRCUIT-PROGRAMMIERUNG

Title (fr)  
ARCHITECTURE DE TOLERANCE DE FAUTES POUR PROGRAMMATION EN-CIRCUIT

Publication  
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Application  
**EP 97937140 A 19970806**

Priority  
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Abstract (en)  
[origin: WO9908186A1] The present invention provides a method and apparatus for providing fault-tolerance for in-circuit programming systems. The invention operates by storing a minimal set of code to initialize the in-circuit programming process in a protected memory (107) so that if the programming process fails, the process can be restarted from the protected memory. This type of fault-tolerance is especially important in systems which allow the code which accomplishes the in-circuit programming to be modified by the in-circuit programming process. One embodiment of the invention provides a multiplexer (110) to selectively switch between a normal boot code sequence (102) and a protected boot code sequence (107), as well as a watchdog timer (122) to monitor the in-circuit programming process to determine whether the process is progressing properly.

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Citation (search report)

- [X] US 5432927 A 19950711 - GROTE JACK A [US], et al
- [X] US 5327531 A 19940705 - BEALKOWSKI RICHARD [US], et al
- [A] US 5247659 A 19930921 - CURRAN MICHAEL W B [GB], et al
- See references of WO 9908186A1

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DE FR GB IT

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