

Title (en)
Flash memory control method

Title (de)
Flash-Speichersteuerverfahren

Title (fr)
Procédé de contrôle de mémoire flash

Publication
EP 1008936 A3 20020327 (EN)

Application
EP 99124043 A 19991209

Priority
JP 35143598 A 19981210

Abstract (en)
[origin: EP1008936A2] A flash memory system (1) comprising a group of memory units (9), each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein, an error detection/correction unit (7) for reading the data written in the group of memory unit and detecting/correcting errors up to a predetermined number, an error judgement section (81, 111) for counting the number of errors detected by the error detection/correction unit (7) and determining the completion of proper data modification of data provided that the number of errors detected by the error detection/correction unit (7) is not greater than the predetermined number. <IMAGE>

IPC 1-7
G06F 11/14; **G11C 11/56**

IPC 8 full level
G06F 11/14 (2006.01); **G06F 12/16** (2006.01); **G11C 11/56** (2006.01); **G11C 16/02** (2006.01); **G11C 16/06** (2006.01); **G11C 29/42** (2006.01); **G06F 11/10** (2006.01)

CPC (source: EP KR US)
G06F 11/1433 (2013.01 - EP US); **G11C 11/5621** (2013.01 - EP US); **G11C 16/02** (2013.01 - KR); **G06F 11/1068** (2013.01 - EP US); **G11C 29/00** (2013.01 - EP US)

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Designated contracting state (EPC)
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DOCDB simple family (publication)
EP 1008936 A2 20000614; **EP 1008936 A3 20020327**; JP 2000173289 A 20000623; KR 100321302 B1 20020318; KR 20000048015 A 20000725; TW 455874 B 20010921; US 6185134 B1 20010206; US RE40252 E 20080422

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EP 99124043 A 19991209; JP 35143598 A 19981210; KR 19990056034 A 19991209; TW 88121627 A 19991210; US 3945905 A 20050120; US 45634099 A 19991208